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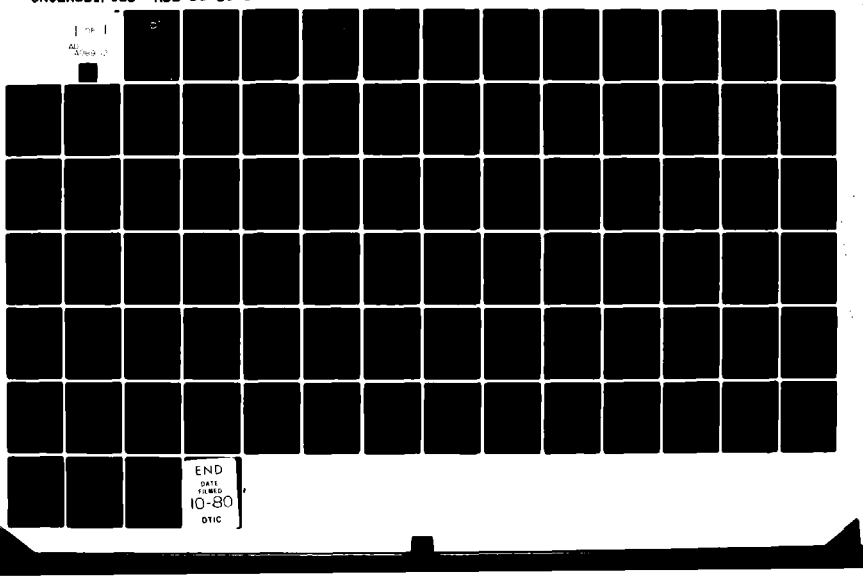

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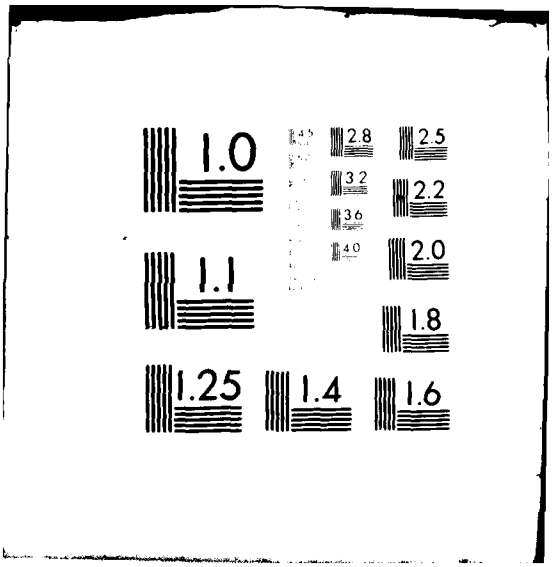
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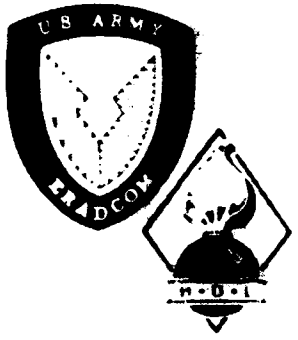
LEVEL II

Nuclear Radiation Effects Data on Large Scale Integrated Circuits

by Roland Polimadei, Harvey Eisen,
and Kelvin Pinero



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This summary tabulates nuclear radiation effects on large scale integrated circuits. This reference can help engineers select components for systems that must survive a given radiation level or evaluate the radiation hardness of previously designed systems. The tables list microprocessors, random access memories, read only memories, programmable read only memories, shift registers, and miscellaneous devices. The data came from government, industry, and IEEE Nuclear and Space Radiation Effects Conference reports.

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FOREWORD

This summary tabulates nuclear radiation effects data on large scale integrated (LSI) circuits. It is intended to be a handy reference to help engineers select components for systems that must survive a given radiation level or evaluate the radiation hardness of previously designed systems. Most of the data in this report were compiled from papers presented at the Annual IEEE Conference on Nuclear and Space Radiation Effects (1971 through 1979). The remainder came from a variety of government and industry reports.

Due to the complexity of testing procedures of LSI devices and the space constraints of a tabular format, not all pertinent data can be presented in this summary. We have attempted to give most of the data needed for assessing the hardness of a given component. The balance of the information can be found in the references.

This summary is divided into an index, six tables of device data, and the references. The index lists the devices in numerical order and cites the tables in which they are listed. The six tables are microprocessors (μP's), random access memories (RAM's), read only memories (ROM's), programmable read only memories (PROM's), shift registers, and miscellaneous devices. Within each table, the devices are arranged numerically. In addition, the μP and RAM tables are subdivided by technology: transistor-transistor logic (TTL), integrated injection logic (I^2L), N-channel metal oxide semiconductor (NMOS), and complementary metal oxide semiconductor (CMOS).

The device technology and the radiation source are described. The number of samples (Smpl size) tested in that radiation source and the results are given next. Because of the complexity of LSI devices, most investigators make functional rather than parametric measurements. For that reason, the results are most often stated here as "functional failure." This is the radiation level at which the first failures (such as loss of stored data, incorrect processing of data, or failure to respond to a command) occurred in the samples tested. When a range of radiation levels is available for the samples tested, that range is given. The terms "transient upset" and "permanent upset" also are used. "Transient upset" means the radiation level at which there was a transient output signal possibly large enough to look like a change of state. "Permanent upset" means the radiation level at which there was a permanent change in some stored data resulting in an incorrect output. Thus, "permanent upset" does not mean that the device was no longer able to function; it means only that some state was changed and had to be reset before correct outputs could be obtained. The seventh column gives the test conditions (such as bias during irradiation or time between irradiation and measurement) and any other pertinent information. The last column lists published (numbered) and unpublished (symbol) references.

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TABLE 1a. CMOS μP'S

Device No.	Technology	Mfr	Smpl size	Radiation source	Results	Test conditions and comments	Ref
TCS010	Si-gate SOS 8-bit CPU	RCA	6	LINAC 50 ns pulse	Transient upset: 5×10^9 rad(Si)/s	Test performed was "register" to "data-in" addition, with fixed input word of alternating ones and zeros. Test began within 30 s after end of irradiation.	1
			6	^{60}Co 5 rad(Si)/s	Functional failure: 2.2×10^4 rad(Si)	Failure to operate.	
TCS074	Si-gate SOS 8-bit CPU	RCA	4	LINAC 40 ns pulse	Transient upset: 8.8×10^9 rad(Si)/s	Test performed was "register" to "data-in" addition, with fixed input word of alternating ones and zeros.	1
			2	1 μs pulse	2.4×10^9 rad(Si)/s	Test began within 30 s after end of irradiation.	
			4	^{60}Co 5 rad(Si)/s	Dose: 4.9×10^3 rad(Si)	Output voltage decreased by 5%.	
					1.3×10^4 rad(Si)	Would not operate.	
1802	Si-gate Bulk 8-bit CPU	RCA	3	^{60}Co 13 to 180 rad (Si)/s	Functional failure: $(3.7 \text{ to } 6.5)10^3$ rad(Si)	V_{DD} = 5 V. All signal and control inputs were connected to logic one or logic zero. Devices were tested after irradiation by placement into development system.	2
			1		3.5×10^4 rad(Si)	Unbiased. Tested as above.	

TABLE 1a. CMOS μP'S (Cont'd)

Device No.	Technology	Mfr	Smpl size	Radiation source	Results	Test conditions and comments	Ref
1802	Si-gate Bulk 8-bit CPU			^{60}Co		During irradiation, devices were biased clocked, or executing program as noted.	3
		HUG	2		Functional failure: 8×10^3 rad(Si)	Executing program, V_{DD} = 5 V. Clock = 100 kHz.	
		RCA	7		$(0.8 \text{ to } 1.5)10^4$ rad(Si)	Clocked at 1 MHz and cleared every 400 μs, or executing program. V_{DD} = 5 V.	
		RCA	1		1.2×10^4 rad(Si)	Developmental SOS, V_{DD} = 5 V, executing program.	
		RCA	6		7×10^3 rad(Si)	Clock = 1 MHz or 10 Vdc. Cleared every 400 μs. V_{DD} = 10 V.	
		RCA	4		$(2 \text{ to } 5)10^5$ rad(Si)	Specially hardened, V_{DD} = 5 V; clocked at 1 MHz and cleared every 400 μs or registers initialized and μP executing program.	
1802DK	Si-gate Bulk 8-bit CPU	RCA	3	^{60}Co	Functional failure: 7×10^3 rad(Si)	During irradiation, devices were biased at V_{DD} = 10 V. All devices were cleared periodically, and either 1 MHz 10 V square wave or 10 Vdc was applied at clock input.	4
CDP1802CD	Si-gate Bulk 8-bit CPU	RCA	2	Flash x-ray 3 ns pulse		Devices were monitored for latchup while being irradiated. Control lines and input and output flags were alternately tied to V_{DD} and then to ground. Biased in static state; V_{CC} = 5 V and 10 V.	5

					Latchup: Observed at ~1.6× 10^9 rad(Si)/s Total dose: 5 rad(Si)	During irradiation, devices were biased at V_{CC} = 10 V. Latchup was not observed for V_{CC} = 5 V.	
CDP1802CD CDP1802D	Si-gate Bulk 8-bit CPU	RCA		LINAC 10 MeV 18 ns pulse		During irradiation, devices were biased at V_{DD} = 5 V. Devices were exercised by RCA COSMAC evaluation kit.	*
			1		Transient upset: 1.2×10^8 rad(Si)/s	Active mode program during irradiation.	
			5		(0.98 to 1.1)10^8 rad(Si)/s	Static mode program during irradiation.	
			5		Latchup: (2.3 to 3)10^8 rad(Si)/s	Latchup current = 400 mA. Static mode program during irradiation.	
			3		Failure: (1.5 to 2)10^4 rad(Si)	Static mode program during irradiation. Full recovery after annealing several hours at 125°C.	
CDP1802CD	Si-gate Bulk 8-bit CPU	RCA	2	^{60}Co 5 rad(Si)/s		During irradiation, devices were operated at V_{DD} = 10 V and clocked at 10 V, 2.3 MHz. Functional test is simple addition, and results are compared with known programmed data.	1
					Functional failure: 9.4×10^3 rad(Si)	Failure to add. Supply current I_{DD} doubled.	

TABLE 1a. CMOS μP'S (Cont'd)

Device No.	Technology	Mfr	Smpl size	Radiation source	Results	Test conditions and comments	Ref
CDP1802D-21	Si-gate Bulk 8-bit CPU	RCA				During irradiation, devices were at nominal bias and performing programmed routines consisting of many different types of instructions. All devices were from single diffusion lot.	†
			5	^{60}Co 100 rad(Si)/s	Functional failure: 8.9×10^{3} rad(Si)	Failure to execute instruction set. Devices were tested during irradiation.	
			18	LINAC 150 ns pulse 37 MeV	Functional failure: 1.8×10^{4} rad(Si)	Total dose accumulated in single pulse. LINAC pulse was triggered at same instant as initiation of instruction set routine. Testing was initiated within 54 μs after LINAC pulse trigger and completed in next 100 ms.	
					Latchup: 19 rad(Si) 1.2×10^{8} rad(Si)/s		
			7	LINAC 1 μs pulse 37 MeV	Functional failure: 2.5×10^{4} rad(Si)	(Same as above.)	

TABLE 1b. NMOS μP'S

Device No.	Technology	Mfr	Smpl size	Radiation source	Results	Test conditions and comments	Ref
F-8	CPU	MOS	10	^{60}Co	Functional failure: 1.7×10^3 rad(Si)	Failure criterion: inability to function or respond to command. Devices were kept in dry ice between irradiation and measurement.	6
F-8	PSU	MOS	10	^{60}Co	1.7×10^3 rad(Si)	V_{DD} = 5 V. V_{GG} = 12 V.	
F-8	CPU (3850)	FAI	10	^{60}Co	1.7×10^3 rad(Si)	V_{DD} = 5 V. V_{GG} = 12 V.	
			10	^{60}Co	No failure at 1×10^4 rad(Si)	Unbiased.	
F-8	PSU (3851)	FAI	10	^{60}Co	1×10^3 rad(Si)	V_{DD} = 5 V. V_{GG} = 12 V.	
			10	^{60}Co	No failure at 1×10^4 rad(Si)	Unbiased.	
F-8	PSU Special radiation-hardened version of 3851	FAI	10	^{60}Co	1×10^4 rad(Si)	V_{DD} = 5 V. V_{GG} = 12 V.	
6800		MOT	3	^{60}Co 13 to 180 rad(Si)/s	Functional failure: 1.7×10^3 rad(Si)	V_{CC} = 5 V. All signal and control inputs were connected to either logic one or logic zero. Devices were tested after irradiation by placement into equipment designed to use them.	2

TABLE 1b. NMOS μP'S (Cont'd)

Device No.	Technology	Mfr	Smpl size	Radiation source	Results	Test conditions and comments	Ref
6800		MOT	3	LINAC 1 μs pulse	Functional failure: (7.7 to 9)10^3 rad(Si)	Devices were irradiated once in active state. After irradiation, data outputs and addresses of test device were compared with those of reference device.	7
6800		NAT	10	^{60}Co	Functional failure: 1×10^3 rad(Si)	Failure criterion: inability to function or respond to command. During irradiation, devices were biased at manufacturer's prescribed burn-in condition.	6
		MOT	10	^{60}Co	Functional failure: 1×10^3 rad(Si)	V_{CC} = 5 V.	
6800P		MOT				During irradiation, V_{CC} = 5 V and programmed routines consisted of many different types of instructions. All devices were from single diffusion lot.	†
			7	^{60}Co 100 rad(Si)/s	Functional failure: 1.8×10^3 rad(Si)	Failure to execute instruction set. Devices were tested during irradiation.	
			11	LINAC 150 ns pulse	Functional failure: 1.9×10^4 rad(Si)	Total dose accumulated in single pulse. LINAC pulse was triggered at same instant as initiation of instruction set routine. Testing was initiated within 54 μs after LINAC pulse trigger and completed in next 100 ms.	

		11	LINAC 1 μs pulse	Functional failure: 1.7×10^4 rad(Si)	Total dose accumulated in single pulse triggered at same instant as initiation of instruction set routine. Testing was initiated within 54 μs after LINAC pulse trigger and completed in next 100 ms.	
8008-1	INT	6	^{60}Co	Functional failure: 2.7×10^3 rad(Si)	During irradiation, devices were clocked and biased according to manufacturer's specifications. Reset and clear signals were applied at 400 μs intervals.	4
8080	INT		^{60}Co 13 to 180 rad(Si)/s		V_{BB} = 5 V. V_{CC} = 5 V. V_{DD} = 12 V. All signal and control inputs were connected to either logic one or logic zero.	2
		3		Functional failure: 490 to 840 rad(Si)	Biased during irradiation.	
		1		1.5×10^4 rad(Si)	Unbiased during irradiation.	
		1		$>3.5\times10^4$ rad(Si)	Unbiased during irradiation.	
	MIL	1		840 rad(Si)	Biased during irradiation.	
	AMD	2		$(2 \text{ to } 2.5)10^3$ rad(Si)	Biased during irradiation.	
		1		2×10^3 rad(Si)	Biased during irradiation.	
		1		$>5\times10^4$ rad(Si)	Unbiased during irradiation.	
	TII	2		1.9×10^3 rad(Si)	Biased during irradiation.	2
		1		2.5×10^4 rad(Si)	Unbiased during irradiation.	
		1		$>5\times10^4$ rad(Si)	Unbiased during irradiation.	

TABLE 1b. NMOS μP'S (Cont'd)

Device No.	Technology	Mfr	Smpl size	Radiation source	Results	Test conditions and comments	Ref
8080		NAT	2		610 to 840 rad(Si)	Biased during irradiation.	2
			2		$>5\times10^4$ rad(Si)	Unbiased during irradiation.	
8080A				^{60}Co	Functional failure:	During irradiation, devices were biased and clocked and then reset and cleared periodically, typically at 400 μs intervals.	4
		NAT	2		700 rad(Si)	Supply current increased by 10% to 3 mA.	
		INT	3		700 rad(Si)	Supply current increased by 10% to 3 mA.	
		AMD	2		3×10^3 rad(Si)	Supply current increased by 10% to 4 mA.	
		NEC	3		5×10^3 rad(Si)		
		TII	2		7×10^3 rad(Si)	Supply current increased by 41% to 22 mA.	
8080A		INT	10	^{60}Co	Functional failure: 1×10^3 rad(Si)	Failure criterion: inability to function or respond to command. V_{BB} = 5 V. V_{CC} = 5 V. V_{DD} = 12 V.	6
			10		1×10^4 rad(Si)	Unbiased during irradiation.	
C8080A		INT		LINAC 1 μs pulse		Devices were irradiated in active state. Starting 40 μs after irradiation, data outputs and addresses of test device were compared with those of reference device.	7

		2		Functional failure: $(2.1 \text{ to } 2.4)10^4$ rad(Si)	Recovered after 6 and 14 min.	
D8080A	INT	4	LINAC 1 μs pulse	Functional failure: $(0.98 \text{ to } 1.8)10^4$ rad(Si)	Devices were irradiated in active state. Starting 40 μs after irradiation, data outputs and addresses of test device were compared with those of reference device.	7
D8080A	INT				During irradiation, devices were at nominal bias and performed programmed routine consisting of many types of instructions.	†
		6	^{60}Co 100 rad(Si)/s	Functional failure: 500 rad(Si)	Failure criterion: failure to execute instruction set. Devices were tested during irradiation. All devices were from one diffusion lot.	
		8	LINAC 150 ns pulse	Functional failure: 9.7×10^3 rad(Si)	Total dose accumulated in single pulse LINAC pulse was triggered at same instant as initiation of instruction set routine. Testing was initiated within 54 μs after LINAC pulse trigger and completed in next 100 ms.	
TMS8080A	TII		LINAC	Cumulative functional failure:	Devices were powered during irradiation, but were not exercised.	‡
		1		945 rad(Si) (one shot)		
		2		$(1.6 \text{ to } 1.9)10^3$ rad(Si) (two shots each)		
		2		$(3.2 \text{ to } 3.8)10^3$ rad(Si) (three shots each)		

TABLE 1b. NMOS μP'S (Cont'd)

Device No.	Technology	Mfr	Smpl size	Radiation source	Results	Test conditions and comments	Ref
TMS8080A		TII	1		No functional failure: 3×10^3 rad(Si)		‡
8080B		INT	1	LINAC 5 μs pulse	Upset: 1.8×10^5 rad(Si)/s Functional failure: 1.5×10^3 rad(Si)	Device was functionally exercised by simple add and compare program, which was recycled until program error occurred or until external reset signal was applied. HALT instructions were placed in all unused memory locations.	8
				200 ns pulse	Latchup: Not observed to 1.8×10^9 rad(Si)/s (no higher tests)		
D8085A		INT				During irradiation, devices were at nominal bias and performed programmed routines consisting of many different types of instructions. All devices were from one diffusion lot.	†
			5	^{60}Co 100 rad(Si)/s	Functional failure: 4.2×10^3 rad(Si)	Failure to execute instruction set. Devices were tested during irradiation.	
			9	LINAC 37 MeV 150 ns pulse	1.7×10^4 rad(Si)	Total dose accumulated in single pulse. LINAC pulse was triggered at same instant as initiation of instruction set routine. Testing was initiated within 54 μs after pulse trigger and completed in next 100 ms.	

		13	LINAC 37 Mev 1 μs pulse	Functional failure: 1.3×10^4 rad(Si)	Total dose accumulated in single pulse. LINAC pulse was triggered at same instant as initiation of instruction set routine. Testing was initiated within 54 μs after trigger and completed in next 100 ms.	
9080	AMD	10	^{60}Co	Functional failure: 1.7×10^3 rad(Si)	Failure criterion: inability to function or respond to command. V_{BB} = -5 V. V_{CC} = 5 V. V_{DD} = 12 V.	6
AM9080ADMB	AMD				V_{BB} = -5 V. V_{CC} = 5 V. V_{DD} = 12 V. Performing programmed routines consisted of many different types of instructions.	†
		6	^{60}Co 100 rad(Si)/s	Functional failure: 2×10^3 rad(Si)	Failure to execute instruction set. Devices were tested during irradiation.	
		3	LINAC 150 ns pulse	Functional failure: 1.6×10^4 rad(Si)	Total dose accumulated in single pulse. LINAC pulse was triggered at same instant as initiation of instruction set routine. Testing was initiated within 54 μs after LINAC pulse trigger and completed in next 100 ms.	

TABLE 1c. TTL μP'S

Device No.	Technology	Mfr	Smpl size	Radiation source	Results	Test conditions and comments	Ref
74S481	4-bit slice STTL	TII				Fifteen test vectors of device under test were compared serially with those for reference device. During irradiation, devices were in static operation at 5 V bias.	9
			5	LINAC 1.4 μs pulse	Transient upset: 1.6×10^{7} rad(Si)/s	Failure criterion: decrease in magnitude of V_{OH} by 0.3 V, such as at Y/AG output.	
					2.4×10^{7} rad(Si)/s	Failure criterion: increase in magnitude of V_{OL} by 0.05 V, such as at D_2 output. At 3×10^{7} rad(Si)/s output, breakup occurs for output levels of 30 to 80 mV. At higher levels, immediate transitions to opposite state occur.	
					Permanent upset: $\sim6\times10^{7}$ rad(Si)/s		
				Flash x-ray 25 ns pulse	Transient upset: $(0.8 \text{ to } 1.1)10^{8}$ rad(Si)/s	Criterion: switching latch.	
					Permanent upset: $(1.0 \text{ to } 1.3)10^{8}$ rad(Si)/s		

AM2901	4-bit slice STTL	AMD				Nominal bias and executing ADD instruction so that output data lines consisted of alternating ones and zeros.	8
			3	LINAC 4 μs pulse	Transient upset: $(0.9 \text{ to } 1.2)10^7$ rad(Si)/s		
			3		Latchup: Not observed at 1.1×10^{10} rad(Si)/s		
			3		Total dose: 2×10^7 rad(Si)	All devices remained operable.	
			3	LINAC 30 ns pulse	Transient upset: $(1 \text{ to } 1.4)10^8$ rad(Si)/s		
AM2901A	4-bit slice STTL	AMD	5	Flash x-ray 20 ns pulse	Transient upset: 3.5×10^{10} rad(Si)/s Latchup: Not observed at this level.	V_{CC} = 5 to 5.5 V. Functionally tested by comparison to known good device; 294 different input combinations were used to exercise each logic cell in both logic one and logic zero conditions at least once. Peak photocurrent: ~10 A.	10
AM2901A	4-bit slice STTL	AMD	10	Sandia reactor		Passive during irradiation. Tested by manufacturer's functional test for proper operation.	§
					1×10^{14} n/cm^2	None failed.	
					4×10^{14} n/cm^2	Seven failed RAM galloping logic ones and zeros test.	

TABLE 1c. TTL μP'S (Cont'd)

Device No.	Technology	Mfr	Smpl size	Radiation source	Results	Test conditions and comments	Ref
AM2901A	4-bit slice STTL	AMD		3	^{60}Co	Devices executed shift instructions at 2 MHz while being irradiated and then were tested according to manufacturer's functional test.	§
					Total dose: 3×10^6 rad(Si)	None failed.	
					6×10^6 rad(Si)	Two failed RAM galloping logic ones and zeros test.	
			3	^{60}Co	Total dose: 9×10^6 rad(Si)	Devices were unbiased during irradiation and then tested as above. None failed.	
AM2901A	4-bit slice LSTTL	AMD	5			Fifteen test vectors of device under test were compared serially with those for reference device. During irradiation, devices were in static operation at bias of 5 V.	9
				LINAC 1.4 μs pulse	Permanent upset: $(0.95 \text{ to } 1.17)10^7$ rad(Si)/s	Most sensitive test vector was OR operation on contents of internal RAM.	
					Transient upset: $\sim4\times10^7$ rad(Si)/s		
				Flash x-ray 25 ns pulse	Permanent upset: $(5.6 \text{ to } 9.5)10^7$ rad(Si)/s		

I3002	Central processing element	INT		Febetron 705 Flash x-ray 30 ns pulse		During irradiations, device inputs were biased so that each arithmetic logic section function of ADD, AND, OR, and EXCLUSIVE OR was active for one set of 2-bit input numbers. Accumulator was set to either 3 (all ones) or 0 (all zeros), and clock was established as either HIGH or LOW.	11
			3		Upset: $(8 \text{ to } 9)10^7$ rad(Si)/s	Data loss in accumulator, in registers for clock in HIGH state, or in registers for clock in LOW state. Thirteen 2-bit memories of each device were loaded with data. After irradiation, data were read out.	
MMI6701D	4-bit slice STTL	MMI				During irradiation, devices were under nominal bias and executing ADD instruction so that output data lines consisted of alternating ones and zeros.	8
			3	LINAC 70 ns pulse	Transient upset: $(1.2 \text{ to } 1.5)10^8$ rad(Si)/s Latchup: Not observed to 4.4×10^8 rad(Si)/s		
			4	4 μs pulse	Transient upset: $(0.5 \text{ to } 4.1)10^7$ rad(Si)/s		

TABLE 1c. TTL μP'S (Cont'd)

Device No.	Technology	Mfr	Smpl size	Radiation source	Results	Test conditions and comments	Ref
MMI6701D	4-bit slice STTL	MMI	1		Latchup: 3.9×10^{8} rad(Si)/s (one device)	I_{CC} increased from 200 to 300 mA, but was restored by interrupting power. Effect was repeatable.	8
			1	LINAC	Cumulative dose: 7×10^{5} rad(Si)	Dose rate used: $<5\times10^{6}$ rad(Si)/s. Sink current I_{OL} degraded by 5%. No change for data-out delay, dc power supply current, output source current, and output voltage levels. Device remained functional.	
			1	WSMR or Sandia reactor	Neutron fluence: 1.5×10^{14} n/cm^2	During irradiation, device was passive and leads were open. Parameter changes: I_{CC}: -6%. I_{OL}: -22%. I_{OH}: -20%. Delay time changes: Output 1: +5%. Output 2: +22%. Output 3: +13%. Output 4: +23%. Device remained functional.	

TABLE 1d. I^2L μP'S

Device No.	Technology	Mfr	Smpl size	Radiation source	Results	Test conditions and comments	Ref
F100-L	16-bit CPU	FER	2	LINAC 1 μs pulse	Transient upset: 5×10^6 rad(Si)/s	Tested dynamically during exposure. V_{CC} = 5 V.	12
			2		Latchup: $>5\times10^9$ rad(Si)/s	Test consisted of multiplying two numbers and monitoring for correct output.	
					Functional failure: 5×10^5 rad(Si)	Program was stored in ROM. Clock rate: 1 kHz.	
			2	VIPER reactor	Functional failure: 1×10^{14} n/cm^2	Passive device irradiation.	
SBP0400	4-bit CPU	TII	-	LINAC 1 to 5 μs pulses	Transient upset: 2×10^7 rad(Si)/s	Injector current was varied over operating range of device.	13
X0400	Prototype of SBP0400 4-bit parallel binary processor	TII				During irradiation, devices were under nominal bias and executing ADD instruction so that output data lines comprised alternating ones and zeros.	8
			1	LINAC 4 μs pulse	Transient upset: 2.1×10^7 rad(Si)/s Latchup: Not observed to 3.7×10^8 rad(Si)/s	Proper switching sequence resumed within 2 μs after radiation pulse. Sequence resumed at 3 μs after 3.7×10^8 rad(Si)/s. No measurable output response occurred below 2×10^7 rad(Si)/s. No surge currents were observed.	

TABLE 1d. I^2L μP'S (Cont'd)

Device No.	Technology	Mfr	Smpl size	Radiation source	Results	Test conditions and comments	Ref
X0400	Prototype of SBP0400 4-bit parallel binary processor	TII	1	LINAC	Functional failure: Cumulative dose: 1.4×10^6 rad(Si)	Device output levels did not degrade, but had improper logic states. No room temp recovery 50 min after 2×10^6 rad(Si). After 48 hr anneal at 200°C, output levels recovered to those measured after irradiation to 3×10^5 rad(Si).	8
			1	WSMR or Sandia reactor	Neutron fluence: 5×10^{11} n/cm^2	I_{OL} degraded by 10%.	
					Functional failure: 1×10^{13} n/cm^2	Nonfunctional for injector current below 5.6 mA.	
					4×10^{13} n/cm^2	Nonfunctional for injector current between 3.2 and 150 mA.	
SBP9900	16-bit CPU	TII	-	LINAC 1 to 5 μs pulses 2.5 MeV	Transient upset: 1×10^8 rad(Si)/s	Injector current was varied over operating range of device.	13
			-	LINAC 20 to 100 ns pulses	4×10^8 rad(Si)/s		
SBP9900	16-bit CPU	TII	2	2.5 MeV	Total dose failure level: 1.2×10^{14} e/cm^2 3×10^6 rad(Si)	Tested on EVM 9900 evaluation board. Injector current level = 523 mA. Clock frequency: 2 MHz. One device had inputs grounded and never recovered. Other device had inputs high and annealed in 45 min.	14

			1		Total dose failure: 1.2×10^{14} e/cm^2 3×10^6 rad(Si)	Device was irradiated with inputs grounded. Larger percentage of decrease of max operating frequency occurred at lower injector current (90 mA) than at higher current (523 mA).	
SBP9900	16-bit CPU	TII	-	LINAC 30 ns pulse	Transient upset: 8.5×10^8 rad(Si)/s	Corresponding outputs of device under test and reference device were compared by logic analyzer. Lack of agreement between outputs indicated failure. Two short-looped programs were repeatedly executed during irradiation until failure was observed.	15
				GaAs laser λ = 0.904 μm 35 to 40 ns pulses	Transient upset: 8.7×10^8 rad(Si)/s		
SBP9900A	16-bit CPU	TII	3	WSMR fast burst reactor		Direct and alternating current and functional measurements were made. Device was passive during irradiation.	16
					Functional failure: (3 to 5)10^{13} n/cm^2	Maximum clock frequency (at I_I = 500 mA) decreased by 10 to 20%. Functional failure was for ac test at frequency = 1 MHz and I_I = 500 mA. No significant change in dc parameters except for degradation in V_{OL}.	
			2	WSMR LINAC 25 ns pulse	Transient upset: 2.5×10^9 rad(Si)/s	During irradiation, devices were tested for 20 different instruction sequences with clock frequency = 1 MHz.	
				80 ns pulse	(1.4 to 1.8)10^9 rad(Si)/s		
				1 μs pulse	1.0×10^9 rad(Si)/s		

TABLE 1d. I^2L μP'S (Cont'd)

Device No.	Technology	Mfr	Smpl size	Radiation source	Results	Test conditions and comments	Ref
SBP9900A	16-bit CPU	TII	4	FX-75 Flash x-ray 25 ns pulse	Survivability test: $>1\times10^{12}$ rad(Si)/s Each device was irradiated five times at this level.	During irradiation, devices were biased at 5 V. I_{OL} decreased by 10 to 20%. All devices passed functional test.	16
			2	^{60}Co 200 rad(Si)/s	Functional failure: (3 to 5)10^6 rad(Si)	Device operated during irradiation and was measured immediately after irradiation. No significant change in dc parameters except for degradation of V_{OL}.	

TABLE 2a. CMOS RAM'S

Device No.	Technology & size (bits)	Mfr	Smpl size	Radiation source	Results	Test conditions and comments	Ref
MM54C200	Metal-gate 256×1 Radiation hardened	NAT	7	^{60}Co	Change in I_{SS}: 2.5 µA preirradiation 15 µA at 10^5 rad(Si) 20 µA at 10^6 rad(Si)	$V_{DD} = V_{IN} = 10$ V. $V_{SS} = 0$ V.	17
					Change in t_{pd}: 220 ns preirradiation 230 ns at 10^5 rad(Si) 255 ns at 10^6 rad(Si)	$V_{DD} = V_{IN} = 10$ V. $V_{SS} = 0$ V. $C_L = 50$ pF.	
MM54C200	256×1	NAT		Flash x-ray 3 ns pulse		During irradiation, devices were biased at normal voltage levels (3 to 14 V) and operated in READ or WRITE mode. No latchup was observed for $V_{CC} < 10$ V.	5
			1		Latchup: 1×10^{10} rad(Si)/s Total dose: 30 rad(Si)	$V_{CC} = 14$ V. Latchup susceptibility was independent of operating mode and input and output logic levels. Latchup current: ~250 mA.	
			1		Transient upset: 1×10^9 rad(Si)/s Total dose: 3 rad(Si)	Lowest total dose level used in this test.	

TABLE 2a. CMOS RAM'S (Cont'd)

Device No.	Technology & size (bits)	Mfr	Smpl size	Radiation source	Results	Test conditions and comments	Ref
MM54C200	256×1	NAT	4	Seifert x-ray 150 kVp 80 to 3000 rad(Si)/min	Functional failure: 1.1×10^{4} rad(Si)	During irradiation, devices were biased at V_{DD} = 5 V and exercised by test pattern generator having 2 µs cycle time. Failure criterion was first occurrence of bit error.	18
MM54C200	Al-gate radiation-hardened process 256×1	NAT		^{60}Co		V_{DD} = 5 V. Devices were in READ mode during irradiation. Stored data were all logic ones or zeros and were read out at 10 kHz during irradiation.	19
			2		Total dose: 1×10^{6} rad(Si)	No difference for stored zeros or ones. Quiescent current increased by one or two orders of magnitude. Access time degraded 5 to 10%.	
MM54C200D	Al-gate radiation hardened process 256×1	NAT	-	Flash x-ray 18 ns pulse	Latchup: None at 2.2×10^{11} rad(Si)/s	During irradiation, devices were biased at V_{DD} = 5 V.	20
					Latchup: None at 8.8×10^{11} rad(Si)/s	Before flash x-ray exposure, devices received 1×10^{14} n/cm^2.	
					Transient upset: 1.8×10^{8} rad(Si)/s	Devices operated at V_{DD} = 5 V and with memory enabled. No previous neutron irradiation.	
					2.0×10^{8} rad(Si)/s	Previous neutron irradiation at 1×10^{14} n/cm^2.	

					5.0×10^{8} rad(Si)/s	Previous neutron irradiation at 1×10^{15} n/cm^2. I_{CC} increased by 2 μA. t_{pd} increased by 10%.	
					1.2×10^{9} rad(Si)/s	Previous neutron irradiation at 1×10^{16} n/cm^2. I_{CC} increased by 25 μA. t_{pd} nearly doubled.	
MM54C929D	1024×1	NAT	4	Febetron 705 Flash x-ray 2 MeV 20 ns pulse	Transient upset: $(3.4 \text{ to } 5)10^{7}$ rad(Si)/s	Exercised using Macrodata. Tested in READ, WRITE, and PAUSE modes. All devices latched up at 5×10^{7} rad(Si)/s in all modes.	21
			4		Permanent upset: $(3.5 \text{ to } 5)10^{7}$ rad(Si)/s		
			4	Febetron 705 2 MeV 50 ns pulse	Functional survivability: 4.7×10^{11} rad(Si)/s		
			10	^{60}Co 5 rad(Si)/s	Failure dose: 3×10^{3} rad(Si)	V_{CC} = 5 V. Five devices had all inputs held high; five had all inputs grounded. Substantial increase in standby current at 1×10^{3} rad(Si). Less than 1 hr between irradiation and measurement.	
MM74C200	256×1	NAT	4	Seifert x-ray 150 kVp 80 to 3000 rad(Si)/min	Functional failure: 1.3×10^{4} rad(Si)	During irradiation, devices were biased at V_{DD} = 5 V and exercised by 2 μs cycle time. Failure criterion was first occurrence of bit error.	18

TABLE 2a. CMOS RAM'S (Cont'd)

Device No.	Technology & size (bits)	Mfr	Smpl size	Radiation source	Results	Test conditions and comments	Ref
MM74C920	Si-gate 256×4	NAT		Flash x-ray 3 ns pulse		During irradiation, devices were biased at V_{CC} = 5 V and operated in READ or WRITE mode.	5
			1		Latchup level: 1×10^9 rad(Si)/s Total dose: 3 rad(Si)	Observed for both READ and WRITE modes. READ mode latchup current was 460 mA. Output high level decreased from 5 to 2 V.	
MM74C929	1024×1	NAT	4	Seifert x-ray 150 kVp 80 to 3000 rad(Si)/min	Functional failure: 3.7×10^3 rad(Si)	During irradiation, devices were biased at V_{DD} = 5 V and exercised by test pattern generator having 2 µs cycle time. Failure criterion was first occurrence of bit error. Standby power dissipation increased by one order of magnitude.	18
CDP1821SCD	SOS 1024×1	RCA	4	Seifert x-ray 150 kVp 80 to 3000 rad(Si)/min	Functional failure: 4×10^3 rad(Si)	During irradiation, devices were biased at V_{DD} = 5 V and exercised by test pattern having 2 µs cycle time. Failure criterion was first occurrence of bit error. Quiescent current began rapid increase at 1×10^3 rad(Si).	18
CDP1821SD	SOS 1024×1	RCA				During irradiation, devices were biased at V_{CC} = 5 V and operated in READ mode.	†
			3	Flash x-ray 20 ns pulse	Transient upset: $(2.3 \text{ to } 2.6)10^6$ rad(Si)/s	Single state change occurred for all devices.	

			4	LINAC 150 ns pulse	Transient upset: $(0.83 \text{ to } 1.0)10^{10}$ rad(Si)/s	Single state change occurred for one device.	
1822	SOS Al-gate 256×4	HUG				During irradiation, devices were biased at V_{DD} = 5 V and operated in various static states.	5
			2	LINAC 50 ns pulse	Upset: $>3.5\times10^{10}$ rad(Si)/s	Data were retained. Above 1×10^{4} rad(Si) accumulated dose, data were lost at 2×10^{10} rad(Si)/s.	
		RCA	4	LINAC 50 ns pulse	Transient upset: $(2.5 \text{ to } 3)10^{10}$ rad(Si)/s Permanent upset: 4×10^{10} rad(Si)/s Functional failure: Will not write: $\sim10^{4}$ rad(Si).	During irradiation, devices were biased at V_{DD} = 5 V and operated in various static states.	
			2	Flash x-ray 3 ns pulse	Dose rate: 3×10^{10} rad(Si)/s	No upset was observed for 10 pulses up to this dose rate.	
CDP1822SCD	SOS 256×4	RCA	4	Seifert x-ray 150 kVp 80 to 3000 rad(Si)/min	Functional failure: 1.1×10^{4} rad(Si)	During irradiation, devices were biased at V_{DD} = 5 V and exercised by test pattern generator having 2 µs cycle time. Failure criterion was first occurrence of bit error.	18
S2222	Si-gate 512×1	MFA	9	^{60}Co	Functional failure: $(3 \text{ to } 4)10^{3}$ rad(Si)	During irradiation, devices were biased at V_{CC} = 10 V. After irradiation, devices were taken to measurement facilities within 15 to 30 min with no bias.	22

TABLE 2a. CMOS RAM'S (Cont'd)

Device No.	Technology & size (bits)	Mfr	Smpl size	Radiation source	Results	Test conditions and comments	Ref
S2222	Si-gate 512×1	MFB	5	^{60}Co	Functional failure: (3 to 4)10^3 rad(Si)	During irradiation, devices were biased at V_{CC} = 10 V. After irradiation, devices were taken to measurement facilities within 15 to 30 min with no bias.	22
CD4061	CMOS 256×1	RCA	8	^{60}Co	Functional failure: 1.5×10^4 rad(Si)	During irradiation, devices were biased at V_{DD} = 10 V. After each irradiation, bias was removed while devices were transported to FAI 5000 IC tester. Devices were tested within 15 to 30 min after each irradiation. (Devices were made after 1973 by high temp gate anneal process.)	22
CD4061	Special Al-gate process 256×1	RCA		^{60}Co		During irradiation, devices were biased at V_{DD} = 5 V and were in READ mode. Stored data were either all ones or all zeros and were read out at 10 kHz during irradiation.	19
			2		Functional failure: 3×10^5 rad(Si)	Stored zeros were read out during irradiation. Quiescent current consumption increased by one order of magnitude. Access time degraded by 25%.	
			2		Functional failure: 1×10^6 rad(Si)	Stored ones were read out during irradiation. Quiescent current increased by two to five orders of magnitude. Access time degraded by 17%.	

CD4061	Si-gate 256×1	RCA	7	^{60}Co	Functional failure: 1.5×10^{4} rad(Si)	V_{DD} = 10 V. Inputs were in various combinations of HIGH and LOW during irradiation. After irradiation, devices were transported to testing within 30 min without bias.	22
CD4061	Si-gate 256×1	RCA		LINAC 10 MeV 18 ns pulse		During irradiation, devices were biased at V_{DD} = 5 V. Test results were independent of test pattern stored and operational mode.	23
			5		Permanent upset: 2.5×10^{8} rad(Si)/s	High reliability devices in active READ mode.	
			5		5.2×10^{8} rad(Si)/s	High reliability devices in standby mode.	
			5		2.2×10^{8} rad(Si)/s	Commercial devices in active READ mode.	
					4.5×10^{8} rad(Si)/s	Commercial devices in standby mode.	
			5		4.3×10^{8} rad(Si)/s	Hardened devices in active READ mode.	
			5		3.9×10^{8} rad(Si)/s	Hardened devices in standby mode.	
			15		Latchup threshold: 4×10^{9} rad(Si)/s	Only 1 sample out of 15 tested latched up below max dose rate (1.4×10^{10} rad(Si)/s) for V_{DD} = 5 V.	
			5	100 ns pulse	Latchup threshold: 1.3×10^{11} rad(Si)/s	High reliability devices. V_{DD} = 5 V.	
			5		1.9×10^{9} rad(Si)/s	High reliability devices. V_{DD} = 10 V.	

TABLE 2a. CMOS RAM'S (Cont'd)

Device No.	Technology & size (bits)	Mfr	Smpl size	Radiation source	Results	Test conditions and comments	Ref
CD4061	Si-gate 256×1	RCA	5	100 ns pulse	Latchup threshold: 2.1×10^{10} rad(Si)/s	Commercial devices. V_{DD} = 5 V.	23
			5		1.4×10^{9} rad(Si)/s	Commercial devices. V_{DD} = 10 V.	
			5		$>1.8\times10^{11}$ rad(Si)/s	Hardened devices. V_{DD} = 5 V.	
			5		3.1×10^{9} rad(Si)/s	Hardened devices. V_{DD} = 10 V.	
CD4061	Si-gate 256×1	RCA	4	Flash x-ray 20 ns pulse		Devices were irradiated under bias. Several addresses with various input patterns were used.	10
					Latchup threshold: 1.8×10^{10} rad(Si)/s Minimum dose: 1.4×10^{3} rad(Si)	V_{CC} = 7 V. Peak photocurrent: ~0.5 A. Accompanied by memory upset.	
CD4061A	256×1 Radiation-hardened version	RCA	20	^{60}Co	Functional failure: 1×10^{6} rad(Si)	Wet-oxide process using 850°C gate-oxide anneal temp. Before and after irradiation, devices were subjected to truth table test sequence. All postirradiation tests were completed within 1 hr after irradiation. V_{DD} = 15 V.	24

CD4061A	256×1	RCA	6	^{60}Co		During irradiation, devices were biased at V_{DD} = 10 V with static input terminal condition and memory data pattern. CHIP-ENABLE input was at 10 V and WRITE/READ input was at 10 V for three devices and 0 V for the other three.	11
					Irradiation 1: 5×10^3 rad(Si)	No change in: power supply current, source current, or sink current. READ access time increased by several percent for V_{DD} = 10 V, but changes were greater for lower V_{DD}.	
					Irradiation 2: 5.4×10^4 rad(Si)	All devices failed in READ mode.	
			4			Devices were in READ mode during irradiation and CHIP-ENABLE and WRITE/READ inputs at 0 V.	
					Irradiation 1: 5×10^3 rad(Si)	Parameter measurements: Power supply current (increased by 5 to 10%). Sink current (increased by 3%). Source current (increased by 10%). READ access time (increased by 10 to 15% for V_{DD} = 10 V, but changes were greater for lower V_{DD}).	
					Irradiation 2: 2.5×10^4 rad(Si)	Parameter changes: Power supply current (doubled). Sink current (large variation). Source current (no change).	

TABLE 2a. CMOS RAM'S (Cont'd)

Device No.	Technology & size (bits)	Mfr	Smpl size	Radiation source	Results	Test conditions and comments	Ref
CD4061A	256×1	RCA	4	^{60}Co		During irradiation, devices were in WRITE mode, CHIP-ENABLE input at 0 V and WRITE/READ input at 10 V.	11
					Irradiation 1: 5×10^{3} rad(Si)	Parameter measurements: Power supply current (increased by 11%). Sink current (no change) Source current (increased by 11%). Read access time (changed by ±10%)	
					Irradiation 2: 2.5×10^{4} rad(Si)	Three devices failed in READ mode.	
			8	Flash x-ray 2 MeV 30 ns pulse	Latchup and permanent upset: 4×10^{8} rad(Si),'s	Failure mechanism for three devices: radiation-induced latchup. No latchup was observed when 50 ohm resistor was used for current limiting. Failure mechanism for three other devices: data loss in internal memory cells. Failure mechanism for remaining two devices: transient upset at data output terminal.	
CD4061A	Wet-oxide 256×1	RCA	20	^{60}Co		Devices were subjected to truth table test sequence, which exercised each transistor in both ON and OFF states. Functional testing was within 1 hr of irradiation.	24
					Functional failure: 1×10^{6} rad(Si)	One device failed.	
					2×10^{6} rad(Si)	One device failed.	

MWS5001	Si-gate SOS 256×1	RCA	4	Seifert x-ray 150 kVp 80 to 3000 rad(Si)/min	Functional failure: 1.2×10^4 rad(Si)	During irradiation, devices were biased at V_{DD} = 10 V and exercised by test pattern generator having 2 μs cycle time. Failure criterion was first occurrence of bit error.	18
MWS5001D	Si-gate SOS 1024×1	RCA	3	^{60}Co 5 rad(Si)/s	Functional failure: 9.8×10^3 rad(Si)	During irradiation, devices operated at V_{DD} = 5 V and clock (1 MHz) = 5 V. Functional exerciser could write and read ones, zeros, or pattern of ones and zeros for each of addressable 1024 bits, in one 2 ms cycle. Input WRITE waveform was compared with output READ waveform. Failure mode: some ones going to zeros observed for alternating logic one and zero data pattern.	1
			1		Functional failure: 2.5×10^4 rad(Si)	During irradiation, device was passive. V_{DD} = 0 V. Clock = 0 V. Failure mode: a few hundred logic ones going to zeros.	
				LINAC 10 MeV		During irradiation, devices were biased at V_{DD} = 5 V. Ones and zeros were loaded into two different addresses and then data were read out. Little room temp annealing at 1000 min for both biased and unbiased devices.	
			2	4 μs pulse	Transient upset: 9×10^8 rad(Si)/s		
			2	500 ns pulse	6.6×10^9 rad(Si)/s		
			4	40 ns pulse	No transient upset observed at 3×10^9 rad(Si)/s		

TABLE 2a. CMOS RAM'S (Cont'd)

Device No.	Technology & size (bits)	Mfr	Smpl size	Radiation source	Results	Test conditions and comments	Ref
MWS5001D	SOS 1024×1	RCA		LINAC 1 μs pulse		All devices were powered during irradiation; V_{CC} = 5V. All functional tests made within minutes of irradiation.	25
			1		3×10^8 rad(Si)/s Cumulative dose: 900 rad(Si)	All logic ones were stored. No bit errors, but device did not function. Supply current = 20 mA.	
			1		3×10^8 rad(Si)/s Cumulative dose: 1.1×10^3 rad(Si)	All logic ones were stored. Bit errors. Device no longer functioned.	
			1		3×10^8 rad(Si)/s Cumulative dose: 994 rad(Si)	All logic ones were stored. Upset occurred, but device operated after being reset. Continued even after irradiation to 3×10^9 rad(Si)/s. Dose = 6400 rad(Si).	
			1		3.5×10^9 rad(Si)/s Cumulative dose: 4.5×10^3 rad(Si)	All logic ones were stored. Bit error.	
			1		2.5×10^8 rad(Si)/s Cumulative dose: >750 rad(Si)	All logic zeros were stored. Device did not load logic ones. Supply current = 10 mA.	
			1		3×10^9 rad(Si)/s Cumulative dose: 6.2×10^3 rad(Si)	All logic zeros were stored. No bit errors occurred.	

MWS5001D MWS5501D	Si-gate SOS 1024×1	RCA		LINAC 10 MeV 18 ns pulse		No distinction was made between these two RAM's. Test results indicate no dependence on pattern type stored.	23
			6		Dose rate: 1×10^{11} rad(Si)/s No permanent upset.	During irradiation, devices were biased at V_{DD} = 5 V in static standby mode.	
			6		6.5×10^{10} rad(Si)/s No permanent upset.	During irradiation, devices were biased at V_{DD} = 5 V in active READ mode.	
			3		2×10^{10} rad(Si)/s No permanent upset.	During irradiation, devices were in either static or active mode at V_{DD} = 2.5 V.	
PD5101	256×4	NEC	8	Seifert x-ray 150 kVp	Functional failure: 3.5×10^{3} rad(Si)	During irradiation, devices were biased at V_{DD} = 5 V and exercised by test pattern generator having 2 µs cycle time. Failure criterion was first occurrence of bit error. Power dissipation increased by three orders of magnitude.	18
MWS5501D	SOS 1024×1	RCA	4	Febetron 705 Flash x-ray 2 MeV 20 ns pulse	Transient or permanent upset: (6 to 7)10^{10} rad(Si)/s	Exercised using Macrodata. Tested in READ, WRITE, and PAUSE modes.	21
			7	Febetron 705 2 MeV Electron beam 50 ns pulse	Functional survivability: 4.7×10^{11} rad(Si)/s		
			10	^{60}Co 27 rad(Si)/s	Functional failure: (7 to 15)10^{3} rad(Si)	V_{CC} = 10 V. Five devices had all inputs held high; five had them all grounded. Substantial standby current increase at 5×10^{3} rad(Si). Less than 1 hr between irradiation and measurement.	

TABLE 2a. CMOS RAM'S (Cont'd)

Device No.	Technology & size (bits)	Mfr	Smpl size	Radiation source	Results	Test conditions and comments	Ref
MWS5501D	SOS 1024×1	RCA		LINAC 1 μs pulse		All devices were powered during irradiation; V_{CC} = 5 V. All functional tests made within minutes of irradiation.	26
			1		Permanent upset: 1×10^9 rad(Si)/s Cumulative dose: 1.1×10^3 rad(Si)	All logic ones were stored. Latchup but resettable by cycling power.	
			1		9×10^9 rad(Si)/s Cumulative dose: 1.7×10^4 rad(Si)	No readout. Device was destroyed. I_{PP} = 40 mA.	
			1		1.2×10^9 rad(Si)/s Cumulative dose: 2.1×10^3 rad(Si)	All logic ones were stored. Device did not reset.	
			1		1.2×10^9 rad(Si)/s Cumulative dose: 1.5×10^3 rad(Si)	All logic zeros were stored. Device did not reset.	
HM6504	4096×1	HAR	4	Seifert x-ray 1.3 to 50 rad(Si)/s	Permanent upset: 7×10^3 rad(Si)	During irradiation, devices were biased at V_{DD} = 5 V and exercised by test pattern generator having 2 μs cycle time. Failure criterion was first occurrence of bit error.	18
6508-2	Si-gate 1024×1	HAR		^{60}Co		During irradiation, devices were biased at V_{DD} = 5 V and were in READ mode. Stored data were either all ones or all zeros and were read out at 10 kHz clock rate during irradiation. Devices were in dry ice ~40 min between irradiation and measurement.	19

			1		Total dose: 5×10^3 rad(Si)	Stored zeros. Quiescent current increased to 10 mA. Access time increased by 5%.	
			1		Total dose: 2×10^3 rad(Si)	Stored ones. Quiescent current increased to 300 µA. Access time increased by 17%.	
6508-5 6508-9	Si-gate 1024×1 Static	HAR	-	Febetron 706 3 ns pulse	Latchup: $\leq 3\times10^9$ rad(Si)/s	V_{CC} = 5 V. Two lots were examined.	27
6508	1024×1 Total dose Radiation-hardened version	HAR	-	Febetron 706 3 ns pulse	Latchup: 2×10^{10} rad(Si)/s Permanent upset: $(1.5 \text{ to } 6)10^9$ rad(Si)/s	V_{CC} = 5 V. No burnout.	
6508-8	Si-gate 1024×1	HAR	4	^{60}Co 5 rad(Si)/s		During irradiation, devices were operated at V_{CC} = 5 V and clock (1 MHz) = 5 V.	1
			1		Functional failure: 8.6×10^3 rad(Si)	Failure modes: ones going to zeros and zeros going to ones. I_{DD} increased by factor of 9.	
			1			During irradiation, device was biased at V_{CC} = 0 V. Clock = 0 V.	
					Functional failure: 6.1×10^4 rad(Si)	Failure mode: zeros going to ones	
HM6508	Si-gate 1024×1	HAR	4	Seifert x-ray 150 kVp 80 to 3000 rad(Si)/min	Functional failure: 1×10^3 rad(Si)	During irradiation, devices were biased at V_{DD} = 5 V and exercised by test pattern having 2 µs cycle time. Failure criterion was first occurrence of bit error.	18

TABLE 2a. CMOS RAM'S (Cont'd)

Device No.	Technology & size (bits)	Mfr	Smpl size	Radiation source	Results	Test conditions and comments	Ref
HMI6508	Si-gate 1024×1	HAR	6	LINAC 10 MeV 18 ns pulse	Latchup and permanent upset: 6×10^7 rad(Si)/s	During irradiation, devices were biased at V_{DD} = 5 V. Test results were independent of operational mode.	23
IM6508	Si-gate 1024×1	ISL	4	Seifert x-ray 150 kVp 80 to 3000 rad(Si)/min	Functional failure: 2.3×10^3 rad(Si)	During irradiation, devices were biased at V_{DD} = 5 V and exercised by test pattern having 2 µs cycle time. Failure criterion was first occurrence of bit error.	18
IM6508	Si-gate 1024×1	ISL	4	LINAC 10 MeV 18 ns pulse	Latchup and permanent upset: 8×10^7 rad(Si)/s	During irradiation, devices were biased at V_{DD} = 5 V.	23
IM6508IDE	Si-gate 1024×1	ISL	2	^{60}Co 5 rad(Si)/s	Functional failure: 1.5×10^3 rad(Si)	During irradiation, devices were biased at V_{CC} = 10 V. Clock (1 MHz) = 10 V. Failure mode: wrong bits. I_{DD} increased by factor of 10.	1
			1		Functional failure: 2.1×10^4 rad(Si)	During irradiation, device was biased at V_{CC} = 1.5 V. Clock (1 MHz) = 1.5 V. Almost complete functional recovery after 46 hr of room temp anneal.	
			2		Functional failure: 3.0×10^4 rad(Si)	During irradiation, devices were passive. V_{CC} = 0 V. Clock = 0 V. Devices were tested immediately after irradiation.	

IM6508MDE	Si-gate 1024×1	ISL	^{60}Co		During irradiation, devices were biased at V_{CC} = 5 V. Clock (1 MHz) = 5 V.	1
		3		Functional failure: 2.7×10^3 rad(Si)	Failure mode: zeros going to ones. Failures occurred suddenly. Supply current increased by factor of 7. Significant annealing when devices were irradiated under zero bias.	
		1		Dose: 7.9×10^4 rad(Si)	During irradiation, device was passive. V_{CC} = 0 V. Clock = 0 V. No bit failures were observed. I_{DD} increased by factor of 4.	
IM6518	Si-gate 1024×1	ISL	Flash x-ray 3 ns pulse		V_{CC} = 5 V. Various logic levels were applied to inputs so that device was biased in READ, WRITE, or intermediate mode during irradiation.	5
		1		Latchup: $(1 \text{ to } 2)10^9$ rad(Si)/s Total dose: 3 to 6 rad(Si)	Latchup was observed in all states. During latchup, device currents range from 150 to 250 mA.	

TABLE 2b. NMOS RAM'S

Device No.	Technology & size(bits)	Mfr	Smpl size	Radiation source	Results	Test conditions and comments	Ref
μPD410D	4096×1	NEC	4	Seifert x-ray 150 kVp 80 to 3000 rad(Si)/min	Failure dose: 1.7×10^3 rad(Si)	During irradation, devices were biased at V_{DD} = 5 V and exercised by test pattern generator having 2 μs cycle time. Failure criterion was first occurrence of bit error.	18
μPD416D	16384×1	NEC	4	Seifert x-ray 150 kVp 80 to 3000 rad(Si)/min	Failure dose: 1.7×10^3 rad(Si)	During irradiation, devices were biased at V_{DD} = 5 V and exercised by test pattern generator having 2 μs cycle time. Failure criterion was first occurrence of bit error.	18
2102A	1024×1	INT	4	Seifert x-ray 150 kVp 80 to 3000 rad(Si)/min	Failure dose: 3×10^3 rad(Si)	During irradiation, devices were biased at V_{DD} = 5 V and exercised by test pattern generator having 2 μs cycle time. Failure criterion was first occurrence of bit error.	18
2102B	1024×1	SIG	4	Seifert x-ray 150 kVp 80 to 3000 rad(Si)/min	Failure dose: 4.5×10^3 rad(Si)	During irradiation, devices were biased at V_{DD} = 5 V and exercised by test pattern generator having 2 μs cycle time. Failure criterion was first occurrence of bit error.	18
MM2102-2MD	1024×1	NAT	4	Febetron 705 Flash x-ray 2 MVp 20 ns pulse	Transient or permanent upset: $(0.95 \text{ to } 1.6)10^8$ rad(Si)/s	Exercised using Macrodata. Tested in READ, WRITE, and PAUSE modes.	21
			5		Functional survivability: 1.6×10^{11} rad(Si)/s		

			10	^{60}Co 1 rad(Si)/s	Failure dose: 1500 rad(Si)	V_{CC} = 5 V. Five devices had all inputs high; five had them all grounded. All survived 500 rad(Si). Less than 1 hr between irradiation and measurement.	
2107B	Si-gate 4096×1 Dynamic	INT	4	Seifert x-ray 150 kVp 80 to 3000 rad(Si)/min	Failure dose: 850 rad(Si)	During irradiation, devices were biased at V_{DD} = 5 V and exercised by test pattern generator having 2 µs cycle time. Failure criterion was first occurrence of bit error.	18
2107B	4096×1	INT	5	Febetron 705 Flash x-ray 20 ns pulse		V_{DD} = 12 V. V_{CC} = 5 V. V_{BB} = -5 V. Real-time monitoring.	28
					Permanent upset range: (5 to 8)10^6 rad(Si)/s Corresponding dose: 0.15 to 0.24 rad(Si)	Clock = 32 kHz.	
					Permanent upset range: (0.5 to 2)10^8 rad(Si)/s Corresponding dose: 1.5 to 5.8 rad(Si)	Clock = 2.5 MHz.	
			9	^{60}Co	Functional failure: 360 to 1100 rad(Si)	Clock = 32 kHz.	

TABLE 2b. NMOS RAM'S (Cont'd)

Device No.	Technology & size (bits)	Mfr	Smpl size	Radiation source	Results	Test conditions and comments	Ref
2114	Si-gate 1024×4 Static	EMM	4	Febetron 706 3 ns pulse	Permanent upset: (0.5 to 1)10^8 rad(Si)/s	V_{CC} = 5 V. All ones or all zeros stored. Irradiated in standby state.	27
2116	16384×1	INT	4	Seifert x-ray 150 kVp 80 to 3000 rad(Si)/min	Functional failure: 900 rad(Si)	During irradiation, devices were biased at V_{DD} = 5 V and exercised by test pattern generator having 2 µs cycle time. Failure criterion was first occurrence of bit error.	18
2147	HMOS 4096×1 Static	INT	5	Febetron 705 Flash x-ray 2 MVp 20 ns pulse	Permanent upset: 1.3×10^7 rad(Si)/s	Exercised by Macrodata. Irradiated in READ, WRITE, and PAUSE cycles.	29
				Febetron 705 Electron beam 50 ns pulse	Functional survivability: $>2.7\times10^{11}$ rad(Si)/s		
			5	^{60}Co 5 rad(Si)/s	Functional failure: 1500 rad(Si)	Incremental irradiations of 500 rad(Si) were done. Functional and parametric measurements were made within 1 hr of irradiation.	
C2147	HMOS 4096×1 Static	INT				During irradiation, devices were biased at V_{CC} = 5 V and operated in READ mode.	†
			3	Flash x-ray 20 ns pulse	Transient upset: 1.0×10^9 rad(Si)/s	Single state change occurred for one device.	

MK4027N	4096×1	MOS	4	Seifert x-ray 150 kVp 80 to 3000 rad(Si)/min	Functional failure: 850 rad(Si)	During irradiation, devices were biased at V_{DD} = 5 V and exercised by test pattern generator having 2 µs cycle time. Failure criterion was first occurrence of bit error.	18
			4	^{60}Co 4×10^3 rad(Si)/min	Functional failure: 1.5×10^3 rad(Si)		
			4	1.5 MeV Van De Graaff accelerator	Functional failure: 1.2×10^3 rad(Si)		
TMS4030	4096×1	TII	4	Seifert x-ray 150 kVp 80 to 3000 rad(Si)/min	Functional failure: 4.1×10^3 rad(Si)	During irradiation, devices were biased at V_{DD} = 5 V and exercised by test pattern generator having 2 µs cycle time. Failure criterion was first occurrence of bit error.	18
TMS4035	1024×1	TII	4	Seifert x-ray 150 kVp 80 to 3000 rad(Si)/min	Functional failure: 3×10^3 rad(Si)	During irradiation, devices were biased at V_{DD} = 5 V and exercised by test pattern generator having 2 µs cycle time. Failure criterion was first occurrence of bit error.	18
			4	^{60}Co 4×10^3 rad (Si)/min	Functional failure: 3.2×10^3 rad(Si)		
			4	1.5 MeV Van de Graaff accelerator 400×10^3 rad (Si)/min	1.7×10^3 rad(Si)		
TMS4050	4096×1	TII	4	Seifert x-ray 150 kVp 80 to 3000 rad(Si)/min	Functional failure: 6.2×10^3 rad(Si)	During irradiation, devices were biased at V_{DD} = 5 V and exercised by test pattern generator having 2 µs cycle time. Failure criterion was first occurrence of bit error.	18

TABLE 2b. NMOS RAM'S (Cont'd)

Device No.	Technology & size (bits)	Mfr	Smpl size	Radiation source	Results	Test conditions and comments	Ref
HYB4060	4096×1	SIE	4	Seifert x-ray 150 kVp 80 to 3000 rad(Si)/min	Functional failure: 2.5×10^3 rad(Si)	During irradiation, devices were biased at V_{DD} = 5 V and exercised by test pattern generator having 2 µs cycle time. Failure criterion was first occurrence of bit error.	18
4096	4096×1	FAI	4	Seifert x-ray 150 kVp 80 to 3000 rad(Si)/min	Functional failure: 800 rad(Si)	During irradiation, devices were biased at V_{DD} = 5 V and exercised by test pattern generator having 2 µs cycle time. Failure criterion was first occurrence of bit error.	18
MK4096P	4096×1	MOS	4	Seifert x-ray 150 kVp 80 to 3000 rad(Si)/min	Functional failure: 1.1×10^3 rad(Si)	During irradiation, devices were biased at V_{DD} = 5 V and exercised by test pattern generator having 2 µs cycle time. Failure criterion was first occurrence of bit error.	18
MK4102N	1024×1	MOS	4	Seifert x-ray 150 kVp 80 to 3000 rad(Si)/min	Functional failure: 2.8×10^3 rad(Si)	During irradiation, devices were biased at V_{DD} = 5 V and exercised by test pattern generator having 2 µs cycle time. Failure criterion was first occurrence of bit error.	18
MK4104P	4096×1	MOS	4	Seifert x-ray 150 kVp 80 to 3000 rad(Si)/min	Functional failure: 1.3×10^3 rad(Si)	During irradiation, devices were biased at V_{DD} = 5 V and exercised by test pattern generator having 2 µs cycle time. Failure criterion was first occurrence of bit error.	18

HYB4116	16384×1	SIE	4	Seifert x-ray 150 kVp 80 to 3000 rad(Si)/min	Functional failure: 2×10^3 rad(Si)	During irradiation, devices were biased at V_{DD} = 5 V and exercised by test pattern generator having 2 µs cycle time. Failure criterion was first occurrence of bit error.	18
MCM4116	16384×1	MOT	4	Seifert x-ray 150 kVp 80 to 3000 rad(Si)/min	Functional failure: 1.3×10^3 rad(Si)	During irradiation, devices were biased at V_{DD} = 5 V and exercised by test pattern generator having 2 µs cycle time. Failure criterion was first occurrence of bit error.	18
TMS4116	16384×1	TII	4	Seifert x-ray 150 kVp 80 to 3000 rad(Si)/min	Functional failure: 2.2×10^3 rad(Si)	During irradiation, devices were biased at V_{DD} = 5 V and exercised by test pattern generator having 2 µs cycle time. Failure criterion was first occurrence of bit error.	18
MK4116P	16384×1	MOS	4	Seifert x-ray 150 kVp 80 to 3000 rad(Si)/min	Functional failure: 2×10^3 rad(Si)	During irradiation, devices were biased at V_{DD} = 5 V and exercised by test pattern generator having 2 µs cycle time. Failure criterion was first occurrence of bit error.	18
SEMI4200	4096×1	EMM				Devices were biased at V_{DD} = 12 V, V_{CC} = 5 V, and V_{BB} = -5 V. Inputs were tied to V_{CC} or ground. Memory was placed in READ, WRITE, or standby state during exposure. Latchup was not observed.	5
			5	Flash x-ray 3 ns pulse	Transient upset: 1×10^9 rad(Si)/s Total dose: 3 rad(Si)	Independent of whether logic one or zero was stored in addressed cell. Upset susceptibility was greatest when voltage level stored on DI line was opposite polarity and level to those in contents of addressed cell.	

TABLE 2b. NMOS RAM'S (Cont'd)

Device No.	Technology & size (bits)	Mfr	Smpl size	Radiation source	Results	Test conditions and comments	Ref
SEMI4200	4096×1	EMM	4	Seifert x-ray 150 kVp 80 to 3000 rad(Si)/min	Functional failure: 1.2×10^3 rad(Si)	During irradiation, devices were biased at V_{DD} = 5 V and exercised by test pattern generator having 2 µs cycle time. Failure criterion was first occurrence of bit error.	18
MCM6604L	4096×1	MOT	4	Seifert x-ray 150 kVp 80 to 3000 rad(Si)/min	Functional failure: 1.2×10^3 rad(Si)	During irradiation, devices were biased at V_{DD} = 5 V and exercised by test pattern generator having 2 µs cycle time. Failure criterion was first occurrence of bit error.	18
MCM6605AL	4096×1	MOT	4	Seifert x-ray 150 kVp 80 to 3000 rad(Si)/min	Functional failure: 2.3×10^3 rad(Si)	During irradiation, devices were biased at V_{DD} = 5 V and exercised by test pattern generator having 2 µs cycle time. Failure criterion was first occurrence of bit error.	18
AM9060	4096×1	AMD	4	Seifert x-ray 150 kVp 80 to 3000 rad(Si)/min	Functional failure: 800 rad(Si)	During irradiation, devices were biased at V_{DD} = 5 V and exercised by test pattern generator having 2 µs cycle time. Failure criterion was first occurrence of bit error.	18
AM9102	1024×1	AMD	4	Seifert x-ray 150 kVp 80 to 3000 rad(Si)/min	Functional failure: 800 rad(Si)	During irradiation, devices were biased at V_{DD} = 5 V and exercised by test pattern generator having 2 µs cycle time. Failure criterion was first occurrence of bit error.	18

AM9140	4096×1	AMD	4	Seifert x-ray 150 kVp 80 to 3000 rad(Si)/min	Functional failure: 1×10^3 rad(Si)	During irradiation, devices were biased at V_{DD} = 5 V and exercised by test pattern generator having 2 µs cycle time. Failure criterion was first occurrence of bit error.	18
4K RAM	4096×1			^{60}Co		During irradiation, devices had either zero gate bias (gate, source, and drain connected together) or gate biased at 12 V with respect to drain and source (connected together). After each irradiation, dry ice was used to minimize annealing. Failures were attributed to threshold voltage shifts in decoder access transistors, causing decoders to be stuck in logic one state.	30
				^{60}Co	Functional failure:		
	A[1]	10			2.7×10^3 rad(Si)	Devices failed: 5	
	B[1]	10			1.7×10^3 rad(Si)	Devices failed: 1	
	C[1]	10			2.7×10^3 rad(Si)	Devices failed: 5	
	D[1]	10			1.7×10^3 rad(Si)	Devices failed: 1	
	E[1]	10			1.7×10^3 rad(Si)	Devices failed: 1	
	F[1]	10			2.7×10^3 rad(Si)	Devices failed: 4	
	G[1]	10			2.7×10^3 rad(Si)	Devices failed: 4	

[1]*Reference 30 conceals identities of these manufacturers: AMD, FAI INT, MOS, MOT, NAT, and TII (ordered alphabetically here).*

TABLE 2c. TTL RAM'S

Device No.	Technology & size (bits)	Mfr	Smpl size	Radiation source	Results	Test conditions and comments	Ref
S82S11F	STTL 1024×1	SIG		Febetron 705 2 MVp 20 ns pulse		During irradiation, devices were exercised by Macrodata MD-104.	21
			5		Transient upset: $(2 \text{ to } 4)10^7$ rad(Si)/s	Devices were irradiated in READ mode. Logic upset is defined to occur when tester TTL input could not sense correct memory output. Stored data may not be scrambled.	
			5		Permanent upset: $(2 \text{ to } 4)10^8$ rad(Si)/s	Devices were irradiated in READ, WRITE or PAUSE mode. Memory data were lost during radiation pulse. Most susceptible when irradiated during active READ/WRITE portion of WRITE cycle.	
			16		Latchup: 2×10^{10} rad(Si)/s	Only two devices latched up. Power supply current increased from 80 to 500 mA. After power was cycled, devices were functional.	
			15	Flash x-ray 2 MeV 50 ns pulse	Functional survivability: $>3\times10^{12}$ rad(Si)/s		
			10	^{60}Co 195 rad(Si)/s	Functional failure: 1×10^6 rad(Si)	During irradiation, devices were biased at V_{CC} = 5 V and all inputs were grounded. One device failed.	
			10	Sandia pulsed reactor	Functional failure: 3×10^{14} n/cm^2	During irradiation, devices had no electrical bias. One device failed. Output drive current decreased by about 30% before functional failure.	

I3101	STTL 16×4	INT	-	Flash x-ray 29 ns pulse	Transient upset: 1.9×10^{8} rad(Si)/s	During irradiation, device was operated under normal voltage; all ones, all zeros, or alternating ones and zeros stored in memory. Monitored during exposure.	28
				Northrop TRIGA	Permanent damage: 1.1×10^{15} n/cm^2		
I3101	STTL 16×4	INT				During irradiation, devices were biased at V_{CC} = 5 V and functionally tested and compared with unirradiated devices.	31
			3	TRIGA reactor	Permanent damage: 7×10^{14} n/cm^2		
			2	Flash x-ray 2 MVp 30 ns pulse	Transient upset: 1.9×10^{8} rad(Si)/s	No latchup was observed at highest test dose rate, 5×10^{10} rad(Si)/s.	
			2	LINAC 4 µs pulse	Transient upset: 1.7×10^{7} rad(Si)/s	No latchup was observed at highest test dose rate, 5×10^{10} rad(Si)/s.	
I3101A	STTL 16×4	INT				During irradiation, devices were biased at V_{CC} = 5 V and functionally tested and compared with unirradiated devices.	31
			3	TRIGA reactor	Permanent damage: 1.4×10^{14} n/cm^2		
			2	Flash x-ray 2 MVp 30 ns pulse	Transient upset: 1.9×10^{8} rad(Si)/s	No latchup was observed at highest test dose rate, 5×10^{10} rad(Si)/s.	
			2	LINAC 4 µs pulse	Transient upset: 3.4×10^{8} rad(Si)/s	No latchup was observed at highest test dose rate, 5×10^{10} rad(Si)/s.	

TABLE 2c. TTL RAM'S (Cont'd)

Device No.	Technology & size (bits)	Mfr	Smpl size	Radiation source	Results	Test conditions and comments	Ref
IM5533A	Au-doped 256×1	ISL	5	LINAC 200 ns pulse	Transient upset: 1.7×10^{8} rad(Si)/s	Tested during irradiation by μP controlled test facility.	8
			2		Total dose: $>3\times10^{7}$ rad(Si) Neutron fluence: 1.3×10^{14} n/cm^2	No operational failure. Output transistors suffered factor-of-five gain loss. (This is considered marginal for proper operation.)	
93425-DM	1024×1 Isoplanar Static	FAI		Febetron 705 2 MVp 20 ns pulse		During irradiation, devices were exercised by Macrodata MD-104.	21
			5		Transient upset: $(0.8 \text{ to } 2)10^{8}$ rad(Si)/s	Devices were irradiated in READ mode. Logic upset is defined to occur when tester TTL input could not sense correct memory output. Memory may not be lost.	
			5		Permanent upset: $(0.8 \text{ to } 4)10^{8}$ rad(Si)/s	Devices were irradiated in READ, WRITE, or PAUSE mode. Memory data were lost during radiation pulse. Most susceptible when irradiated during active READ/WRITE portion of WRITE cycle.	
			5	Flash x-ray 2 MVp 50 ns pulse	Functional survivability: $>3\times10^{12}$ rad(Si)/s	Memory was scrambled, but could be rewritten, and devices functionally operated after irradiation.	

10	^{60}Co 195 rad(Si)/s	Functional failure: 1×10^6 rad(Si)	During irradiation, devices were biased at V_{CC} = 5 V and all inputs were grounded. Seven devices failed.
10	Sandia pulsed reactor	Functional failure: 3×10^{14} n/cm^2	During irradiation, devices had no electrical bias. Output drive currents decreased by about 30% before functional failure. One device failed.

TABLE 2d. PMOS RAM'S

Device No.	Technology & size(bits)	Mfr	Smpl size	Radiation source	Results	Test conditions and comments	Ref
I1101	Si-gate PMOS 256×1 Static	INT				During irradiation, devices were biased at normal operating voltage, and two randomly selected bits were monitored. All address lines but one were dc wired.	32
			-	LINAC 50 ns to 4.5 μs	Dose rate: 1.7×10^{7} to 2×10^{9} rad(Si)/s	No radiation-induced change of state observed.	
			6	Flash x-ray 2 MeV 30 ns pulse		An alternating logic one and zero pattern was loaded into entire array. Single bit was monitored during exposure while device was in READ mode. After irradiation, entire memory was scanned and compared with preirradiation pattern.	
					Dose rate: 1×10^{11} rad(Si)/s	No radiation-induced change of state was observed for single-bit test.	
					2.5×10^{8} rad(Si)/s	All bits were scanned. All six devices had lost some stored information.	
I1101	Si-gate PMOS 256×1 Static	INT	4	^{60}Co 1×10^{5} rad(Si)/hr	Functional failure: 2×10^{4} rad(Si)	During irradiation, devices were biased and tested at V_{DD} = -10 V and V_{CC} = 5 V. Tested during irradiation.	31
			-	Flash x-ray 2 MVp 30 ns pulse	Transient upset: 2×10^{8} rad(Si)/s	Latchup was not observed at highest test dose rate, 5×10^{10} rad(Si)/s.	
			-	LINAC 4 μs pulse	Transient upset: 1.1×10^{8} rad(Si)/s	Latchup was not observed at highest test dose rate, 5×10^{10} rad(Si)/s.	

TABLE 2e. I^2L RAM'S

Device No.	Technology & size(bits)	Mfr	Smpl size	Radiation source	Results	Test conditions and comments	Ref
93481	4096×1	FAI	4	Seifert x-ray 150 kVp 80 to 3000 rad(Si)/min	Functional failure: 1.5×10^4 rad(Si)	During irradiation, devices were biased at V_{DD} = 5 V and exercised by test pattern generator having 2 μs cycle time. Failure criterion was first occurrence of bit failure. Standby power dissipation began to increase at 2.0×10^4 rad(Si).	18
			4	^{60}Co 4×10^3 rad(Si)/min	Functional failure: 2.0×10^4 rad(Si)		
			4	1.5 MeV Van de Graaff accelerator 4×10^5 rad(Si)/min	Functional failure: 1.9×10^4 rad(Si)		

TABLE 2f. MNOS RAM'S

Device No.	Technology & size(bits)	Mfr	Smpl size	Radiation source	Results	Test conditions and comments	Ref
SR2256	Si-bulk MNOS 64×4 Static Electrically alterable Nonvolatile	SPR	15	Febetron 705 Flash x-ray 50 ns pulse		During irradiation, devices were biased at ±15 V and were exercised by Macrodata MD-104 LSI test system. Flash x-ray burst was synchronized to any point within operational cycle.	33
					Transient upset: 4×10^{8} rad(Si)/s	Device in READ mode. Flash x-ray pulse was applied 1 μs before start of logic one or logic zero data output signal. Recovery time was one READ cycle.	
					2.4×10^{11} rad(Si)/s	Device was in CLEAR/WRITE mode. Radiation pulse was applied at start of memory enable signal (most sensitive condition for upset). Errors observed in following READ period were result of decreased peak output voltage levels of data output signals. No false data were written into or out of memory.	
					1.0×10^{12} rad(Si)/s	Device operated in PAUSE mode during irradiation. Minimum recovery time was 80 μs. No loss of preirradiation memory data.	
			1		1.3×10^{12} rad(Si)/s	Memory electrical timing parameters were adjusted to obtain proper post-irradiation operation. No memory loss.	
			1		2.0×10^{12} rad(Si)/s	Device was destroyed.	

6	^{60}Co 77 rad(Si)/s		During irradiation, devices operated in (1) CLEAR/WRITE/READ cycle, where memory was continuously cycled through all operating modes at max cycle rate, (2) PAUSE or WAIT mode, or (3) passive state (no power applied).
		Dose: 2.0×10^5 rad(Si)	Read-access time degraded. Timing signals were adjusted to maintain proper device operation. Test results were independent of device operation during irradiation.
		Functional failure: 3.0×10^5 rad(Si)	All devices failed because of radiation-induced gate threshold shifts in PMOS peripherals.

TABLE 3. ROM'S

Device No.	Technology & size (bits)	Mfr	Smpl size	Radiation source	Results	Test conditions and comments	Ref
1833	CMOS 1024×8	RCA	2	^{60}Co 13 to 180 rad(Si)/s	Functional failure: 5.5×10^{3} rad(Si)	During irradiation, devices were powered by Duracell batteries. All signal and control inputs were connected to logic one or logic zero. Devices were tested after irradiation by placement into development system.	2
IM5625	TTL 512×8	ISL	5	Flash x-ray 20 ns pulse	Dose rate: 2.5×10^{10} rad(Si)/s Latchup and upset: Not observed	During irradiation, devices were biased at V_{CC} = 5 V, and results were compared with those of unirradiated device. Peak photocurrent: ~0.5 A.	10
IM6312	Si-gate CMOS 1024×12	ISL		^{60}Co 5 rad(Si)/s		Functional test was to monitor five 12-bit words stored at specific addresses. Words could comprise all ones, all zeros, or alternating ones and zeros.	1
			2		Functional failure: 2.0×10^{4} rad(Si)	During irradiation, device was passive (V_{CC} = 0 V).	
			2		Functional failure: 2.4×10^{3} rad(Si)	During irradiation, devices were biased at V_{CC} = 10 V and clock (1 MHz) = 10 V.	
SMS8228	STTL 1024×4	SMS	10	TRIGA reactor	Permanent damage fluence: 2×10^{14} n/cm^2	During irradiation at room temp, devices were biased at V_{CC} = 5 V and functionally tested, and results were compared with those of unirradiated device. Performance of internal cells was measured in groups of 4-bit words.	31
			-	Flash x-ray 2 MeV 30 ns pulse	Transient upset: 2×10^{7} rad(Si)/s	Latchup was not observed at highest test dose rate, 5×10^{10} rad(Si)/s	
			-	LINAC 4 μs pulse	Transient upset: 2×10^{6} rad(Si)/s	Latchup was not observed at highest test dose rate, 5×10^{10} rad(Si)/s.	

TABLE 4. PROM'S

Device No.	Technology & size (bits)	Mfr	Smpl size	Radiation source	Results	Test conditions and comments	Ref
ER3400	MNOS EAROM 4096×1	GEN	-	Febetron 705 Flash x-ray 20 ns pulse	Transient upset: READ mode: 1.1×10^{8} rad(Si)/s WRITE mode: 3.1×10^{8} rad(Si)/s	Radiation was applied 200 ns before start of data output pulse in READ mode and at start of write setup time in WRITE mode. V_{GG} = -30 V. V_{SS} = 5 V. V_{DD} = -12 V.	34
				2 MeV Electron beam 50 ns pulse	Functional failure: $>9.0\times10^{11}$ rad(Si)/s	Device was in PAUSE mode. No functional failure. No loss of data, but increase in READ access time.	
			24	^{60}Co 22 rad(Si)/s	Functional failure:	Devices were tested under following conditions:	
					$(2 \text{ to } 4)10^{4}$ rad(Si)	Continuous READ, continuous PAUSE, or cycling through CLEAR/WRITE/READ mode.	
					$(4 \text{ to } 6)10^{4}$ rad(Si)	Unbiased (no power applied).	
I3601	STTL 256×4	INT	3	Flash x-ray 30 ns pulse	Transient upset: 1×10^{7} rad(Si)/s	During irradiation, each device had different stored pattern (all ones, all zeros, or alternating ones and zeros). All open-collector outputs were tied to 5 V supply by 1 kilohm resistor. Address inputs were driven by 8-bit binary counter.	28

TABLE 4. PROM'S (Cont'd)

Device No.	Technology & size (bits)	Mfr	Smpl size	Radiation source	Results	Test conditions and comments	Ref
I3624	STTL 512×8	INT				During and after irradiation, devices were exercised by programming two different words into two different memory locations and then cycling between these locations to monitor for correct data output.	8
			1	LINAC 4 μs pulse	Transient upset: 2.3×10^{7} rad(Si)/s		
					6.1×10^{7} rad(Si)/s	Outputs saturated in zero state.	
					Latchup: Not observed at 1.1×10^{10} rad(Si)/s	No internal data were altered up to 1.1×10^{10} rad(Si)/s.	
			1	LINAC	Cumulative dose: 1×10^{7} rad(Si)	Device remained functional. I_{OL} decreased by 15%, and address-to-output delay decreased by 14%.	
6340D	STTL 512×8	MMI				Exercised during and after radiation pulse by programming two different words into two different memory locations and then cycling between these locations to monitor for correct data output.	8
			1	LINAC 4 μs pulse	Transient upset: 9.2×10^{6} rad(Si)/s	Three of four outputs did not switch properly during radiation pulse. Recovery occurred in ~1 μs.	
					1×10^{8} rad(Si)/s	All outputs saturated in zero state.	

					Latchup: Not observed at 4×10^8 rad(Si)/s	Recovery time = 8 µs. No internal data were altered over range 5×10^6 to 4×10^8 rad(Si)/s.	
			1	LINAC	Cumulative dose: 1×10^6 rad(Si)	No measurable degradation in electrical parameters.	
			1	WSMR or Sandia reactor	Neutron fluence: 1.5×10^{14} n/cm^2	Device was passive and leads were open. Device remained functional. I_{OL} decreased by 72%, which is barely adequate to drive one gate.	
NCM7040	MNOS EAROM 256×1	NIT	7	Febetron 705 Flash x-ray 20 ns pulse	Transient upset: 2×10^7 rad(Si)/s	Radiation was applied at start of data output pulse in READ mode or at start of write setup time in WRITE mode. WRITE mode threshold was slightly higher. Device recovery time (for READ mode) ranged from 0.2 to 25 µs. V_{SS} = ±15 and 5 V.	34
					Functional failure: $>7\times10^{11}$ rad(Si)/s	Devices were irradiated while in PAUSE or WAIT period. Devices still functioned after recovery period.	
			3	^{60}Co 28 rad(Si)/s	Functional failure: 1.7×10^4 rad(Si)	Device was either cycling through all of its operational modes or in READ mode.	
					3.8×10^4 rad(Si)	Device was operating in PAUSE mode only.	

TABLE 5. SHIFT REGISTERS

Device No.	Technology & size (bits)	Mfr	Smpl size	Radiation source	Results	Test conditions and comments	Ref
1402	PMOS Si-gate 256×4 Dynamic	INT	5	^{60}Co 30 rad(Si)/s	Permanent damage: (1.4 to 15)10^4 rad(Si)	During irradiation, V_{DD} = -10 V, and V_{CC} = 5 V. Clock rate = 40 kHz.	31, 35
			5	LINAC 50 ns pulse	Permanent upset: 3 rad(Si)	Bias during irradiation was not given. Upset depended on clock rate and dose received.	
1402	PMOS 256×4 Dynamic	INT	-	Flash x-ray 2 MeV 30 ns pulse	Permanent upset: 1.0 rad(Si)	During irradiation, device was operated by inputting alternate ones and zeros.	32
				LINAC 0.05 to 4 µs pulses	1.7 to 4.5 rad(Si)	Device was continuously monitored for transient response and permanent upset.	
				TRIGA 10 ms pulse	1.5 to 1.9 rad(Si)		
1406	PMOS 100×2 Dynamic	INT	-	Flash x-ray 2 MeV 30 ns pulse	Permanent upset: 1.2 rad(Si)	During irradiation, device was operated by inputting alternate ones and zeros. Device was continuously monitored for transient response and permanent upset.	32
				TRIGA reactor 10 ms pulse	Permanent upset: 2.2 rad(Si)		
DRA2001	TTL 256×2	TII	3	TRIGA reactor 10 ms pulse	Permanent damage: 5×10^{14} n/cm^2	During irradiation, devices were biased at V_{BB} = 2.5 V and V_{CC} = 5 V. Devices were tested after irradiation by being compared with control device.	31

			5	Flash x-ray 2 MeV 30 ns pulse	Transient upset: 2×10^8 rad(Si)/s	During irradiation, devices were biased and tested at V_{BB} = 2.5 V and V_{CC} = 5 V and tested as function of various stored data patterns.	
			5	LINAC 4 µs pulse	Transient upset: 2×10^8 rad(Si)/s		
2812	PMOS 32×8 FIFO	AMD	2	^{60}Co 13 to 180 rad(Si)	Functional failure: $>8\times10^3$ rad(Si)	Devices were unbiased during exposure. Devices were tested after irradiation by placement into equipment that had been designed to use this register.	2
			2		Functional failure: 4×10^3 rad(Si)	Devices were biased at operating voltage during exposure and tested as above.	
TMS3003	MOS 100×2 Dynamic	TII	-	Flash x-ray 30 ns pulse	Permanent upset: 1.5 rad(Si)	During irradiation, device was operated by inputting ones and zeros. Device was continuously monitored for transient response and permanent upset.	32
				LINAC 0.05 to 4 µs pulses	0.7 to 2.2 rad(Si)		
				TRIGA 10 ms pulse	2.1 rad(Si)		
3300	PMOS 25×1 Static	FAI	-			During irradiation, device was operated and continuously monitored for transient response and permanent upset.	32
				Flash x-ray 2 MeV 30 ns pulse	Permanent upset: 1×10^9 rad(Si)/s	Peak output photoresponse was 2 V. Loss of stored information.	
				TRIGA reactor 20 ms pulse	Permanent upset: 1×10^6 rad(Si)/s	Loss of stored information.	

TABLE 5. SHIFT REGISTERS (Cont'd)

Device No.	Technology & size (bits)	Mfr	Smpl size	Radiation source	Results	Test conditions and comments	Ref
3303	MOS 25×2 Dynamic	FAI	-	Flash x-ray 2 MeV 30 ns pulse	Permanent upset: 3.0 rad(Si)	During irradiation, device was operated by inputting ones and zeros. Device was continuously monitored for transient response and permanent upset.	32
				LINAC 0.05 to 4 μs pulses	4.0 to 7.0 rad(Si)		
				TRIGA reactor 10 ms pulse	6.0 rad(Si)		

TABLE 6. MISCELLANEOUS DEVICES

Device No.	Technology	Mfr	Smpl size	Radiation source	Results	Test conditions and comments	Ref
SN54S181	STTL	TII	6	TRIGA reactor	Permanent damage: 2.1×10^{14} n/cm^2	Arithmetic logic unit. During irradiation, devices were biased at V_{CC} = 5 V. After irradiation, devices were tested at maximum fanout and results were compared with those of control device.	31
			-	Flash x-ray 2 MeV 30 ns pulse	Transient upset: 1.5×10^{8} rad(Si)/s		
			-	LINAC 4 µs pulse	Transient upset: 2×10^{7} rad(Si)/s		
82S100	STTL	MMI	4	Flash x-ray 20 ns pulse	Latchup: 2×10^{9} rad(Si)/s No transient upset at this level	Field progammable logic array (FPLA). During irradiation, devices were biased at V_{CC} = 4.5 to 6.6 V. Immediately after irradiation, devices were tested for 44 different input combinations and results were compared with those of control device.	10
AM2909	STTL	AMD	5	Flash x-ray 20 ns pulse	Transient upset: 2.5×10^{10} rad(Si)/s Latchup: Not observed	Microprogram sequencer. During irradiation, devices were biased at V_{CC} = 5 V. Devices were functionally tested for 300 different input combinations immediately after pulse, and results were compared with control device.	10

TABLE 6. MISCELLANEOUS DEVICES (Cont'd)

Device No.	Technology	Mfr	Smpl size	Radiation source	Results	Test conditions and comments	Ref
AM2910	LSTTL	AMD				Microprogram controller. Fifteen test vectors of devices under test were compared serially with those for reference device. During irradiation, devices were in static operation at 5 V bias.	9
			5	LINAC 1.4 μs pulse	Permanent upset: 1.2×10^{7} rad(Si)/s	One word of 5×12 stack register ended up with wrong bit.	
			5	Flash x-ray 25 ns pulse	Transient upset: 7×10^{7} rad(Si)/s		
					Permanent upset: 1.4×10^{8} rad(Si)/s		
S3000	TTL	INT				Two-bit slice microcomputer system. During irradiation, device was executing low-pass digital filter algorithm.	28
			1	Febetron 705 Flash x-ray 29 ns pulse	Functional failure: 1×10^{8} rad(Si)/s	Failure to execute digital function properly.	
			1	TRIGA Mark F reactor	Failure fluence: 3×10^{14} n/cm^2 Gamma dose: 1.1×10^{5} rad(Si)	Computation error: all data output was zero. Four minutes after irradiation, device began to respond, and at 5 min device was computing without error.	

3001	TTL	INT	2	Febetron 705 Flash x-ray 29 ns pulse	Transient upset: 8×10^{7} rad(Si)/s	Microprogram control unit. Internal registers were set to various patterns. Most susceptible state was HIGH condition with clock LOW during pulse. Devices were monitored during exposure.	28
3003	STTL	INT		Febetron 705 Flash x-ray 50 ns pulse		Look-ahead carry generator. During irradiation, devices were biased in static condition with outputs either HIGH or LOW. Devices were tested immediately after irradiation. Failure was defined as change of at least 1.4 V for output voltage.	36
			3		Transient upset: 7×10^{8} rad(Si)/s	Logic one state failure level.	
					6×10^{8} rad(Si)/s	Logic zero state failure level.	
IM6402	Si-gate CMOS	ISL	2	^{60}Co 5 rad(Si)/s		Universal asynchronous receiver-transmitter (UART). During irradiation, devices were passive, and all inputs were grounded. Functional test comprised inputting eight words and transmitting converted data through UART to comparator.	1
					Degradation dose: 4×10^{4} rad(Si)	Supply current increased by factor of 10. Threshold voltage decreased by 40%.	
					Functional failure: $>5\times10^{4}$ rad(Si)		
9404	I^2L	FAI	1	LINAC 30 ns pulse	Transient upset: 6×10^{8} rad(Si)/s	Microprogram sequencer. Device was exercised through sequence test that checked integrity of data in all internal registers during and after radiation pulse. Certain bits of program counter register changed to logic zero during pulse.	15
			1	GaAs laser λ = 0.904 µm 35 ns pulse	Transient upset: 6×10^{8} rad(Si)/s		

TABLE 6. MISCELLANEOUS DEVICES (Cont'd)

Device No.	Technology	Mfr	Smpl size	Radiation source	Results	Test conditions and comments	Ref
9408	I^2L	FAI	1	LINAC 30 ns pulse or GaAs laser λ = 0.904 μm 35 ns pulse	Transient upset: 6×10^8 rad(Si)/s	Microprogram sequencer. Device was exercised through sequence of tests that checked integrity of data in all internal registers during and after radiation pulse. First upsets were change of certain bits of program counter register to logic zero.	15
9408	I^2L	FAI	2	WSMR fast burst reactor	Failure fluence: 10^{14} n/cm^2	Microprogram sequencer. Functionally tested by using microcomputer or functional and dc parametric tests with Tektronix S3260. Both devices survived 3×10^{13} n/cm^2.	37
			3	^{60}Co	Functional failure: 3×10^5 rad(Si)	Functional and dc parametric tests done with Tektronix S3260. All devices survived 1×10^5 rad(Si).	
			2	LINAC 30 ns pulse	Permanent upset: 6×10^8 rad(Si)/s	Program counter data were scrambled. Cause was upset of master reset input buffer.	
			2	LINAC 100 ns pulse	2.9×10^8 rad(Si)/s		

MCM14512	CMOS 8-channel	MOT	1	^{60}Co	Functional failure: 1.5×10^{4} rad(Si)	Data selector. During irradiation, device was biased at V_{DD} = 10 V. Bias was removed after irradiation while device was transported to FAI 5000 IC tester. Tests were performed within 15 to 30 min after irradiation. (Device was made after 1973, and high temp gate anneal process was used.)	22
SCL14512	CMOS 8-channel	SOL	1	^{60}Co	Functional failure: 2×10^{4} rad(Si)	Data selector. During irradiation, device was biased at V_{DD} = 10 V. Bias was removed after irradiation while device was transported to FAI 5000 IC tester. Tests were performed within 15 to 30 min after irradiation. (Device was made after 1973, and high temp gate anneal process was used.)	22
MC14559	CMOS 512×1	MOT	5	^{60}Co	Functional failure: 7×10^{3} rad(Si)	Successive approximation register. During irradiation, devices were biased at V_{DD} = 10 V. Bias was removed while devices were transported to FAI 5000 IC tester. Tests were performed within 15 to 30 min after irradiation.	22

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SYMBOLS

Technology

CMOS	Complementary metal oxide semiconductor
CPU	Central processing unit
EAROM	Electrically alterable read only memory
FPLA	Field programmable logic array
HMOS	High density metal oxide semiconductor
IC	Integrated circuit
I^2L	Integrated injection logic
LSTTL	Low power Schottky transistor-transistor logic
MNOS	Metal nitride oxide semiconductor
MOS	Metal oxide semiconductor
NMOS	N-channel metal oxide semiconductor
PMOS	P-channel metal oxide semiconductor
PSU	Programmable storage unit
SOS	Silicon on sapphire
STTL	Schottky transistor-transistor logic
TTL	Transistor-transistor logic
UART	Universal asynchronous receiver-transmitter

Manufacturer

AMD	Advanced Micro Devices
EMM	EMM/SEMI, Inc.
FAI	Fairchild
FER	Ferranti
GEN	General Instruments
HAR	Harris
HUG	Hughes
INT	Intel Corp.
ISL	Intersil, Inc.
MFA	Manufacturer A
MFB	Manufacturer B
MIL	Military version
MMI	Monolithic Memories, Inc.
MOS	Mostek Corp.
MOT	Motorola
NAT	National Semiconductor

Manufacturer (Cont'd)

NEC	Nippon Electric Co., Ltd.
NIT	Nitron
SIE	Siemens
SIG	Signetics
SMS	Scientific Microsystems
SOL	Solid State
SPR	Sperry Rand
TII	Texas Instruments, Inc.

Source

kVp	Kilovolts peak
LINAC	Linear accelerator
MVp	Megavolts peak
WSMR	White Sands Missile Range, NM

Test conditions

C_L	Load capacitance
DI	Dielectric isolation
FIFO	First in, first out
I_{CC}	Quiescent supply current
I_{DD}	Supply current
I_I	Input current
I_{OH}	Current of output in HIGH state
I_{OL}	Current of output in LOW state
I_{pp}	Primary photocurrent
t_{pd}	Propagation delay time
V_{BB}	Supply voltage to base
V_{CC}	Supply voltage to collector
V_{DD}	Supply voltage to drain
V_{GG}	Supply voltage to gate
VIN	Input voltage
V_{OH}	Voltage of output in HIGH state
V_{OL}	Voltage of output in LOW state
V_{SS}	Supply voltage to source

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